IN THE CLAIMS:

1. (Previously Presented) A microprocessor for processing instructions, comprising:

a plurality of clusters for receiving the instructions, each of the clusters having a plurality of functional units for executing the instructions; and

a plurality of register sub-files each having a plurality of registers for storing data for executing the instructions, wherein the register sub-files each have a same number of registers;

wherein each of the clusters is associated with corresponding one of the register sub-files, and each of the register sub-files is associated with a corresponding one of the clusters, so that an instruction dispatched to a cluster is executed by accessing registers in a register sub-file associated with the cluster to which the instruction is dispatched, and wherein each of the register sub-files has one write port to which a corresponding cluster sends data to be written into registers in a register sub-file associated with the corresponding cluster.

2-3. (Canceled)

4. (Original) The microprocessor of claim 1, further including a register-renaming unit for renaming target registers in an instruction with registers in a register sub-file associated with a cluster to which the instruction is dispatched.

5. (Original) The microprocessor of claim 4, wherein the register-renaming unit identifies a register to be used to store a value named by a target register in the instruction.

6. (Original) The microprocessor of claim 4, further including issue-queue units each of which is associated with a corresponding one of the clusters, an issue-queue unit

holding instruction renamed by the register-renaming unit until the renamed instruction is issued to be executed in a cluster associated with the issue-queue unit.

7. (Original) The microprocessor of claim 6, wherein each of the issue-queue units holds state identifying which instructions need to be executed.

8. (Original) The microprocessor of claim 6, further including an instruction dispatch mechanism for determining which of the clusters each instruction is dispatched to.

9. (Original) The microprocessor of claim 8, wherein the instruction dispatch mechanism controls the issue-queue units to determine which of the instructions need to be executed.

10-14. (Canceled)

15. (Previously Presented) A method for processing instructions in a microprocessor, comprising the steps of:

providing clusters each having functional units for executing the instructions;

dividing a register file into a plurality of register sub-files each having registers to store data for executing the instructions, wherein the register sub-files each have a same number of registers;

associating each of the register sub-files with corresponding one of the clusters;

providing one write port for each of the register sub-files so that a cluster associated with a register sub-file sends data to be written to a write port of the register sub-file;

selecting a cluster to which an instruction is dispatched;

renaming target registers in the instruction with registers in a register sub-file associated with the selected cluster; and

dispatching the instruction to the selected cluster wherein the instruction is executed by functional units.

16-17. (Canceled)

18. (Original) The method of claim 15, wherein the renaming step includes identifying a register in a register sub-file to be used to store value named by a target register in the instruction.

19. (Original) The method of claim 15, further including holding an instruction renamed in the renaming step until the renamed instruction is issued to be executed by a cluster.